IN THE CLAIMS

Claim 1 (previously presented): A circuit for minimizing the effects of ESD events on data cells, comprising:

a clamp circuit with an input and output to clamp after an ESD event;

a delay circuit with an input and an output to delay during said ESD event; and

the coupled clamp circuit and delay circuit operable to keep voltage to one or a plurality of input nodes coupling the output of the delay circuit to a data cell below a predetermined threshold.

Claim 2 (original): The circuit for minimizing the effects of ESD events on data cells of Claim 1, further comprising:

the delay circuit being operable to dictate the operation during transient conditions of an ESD event;

the clamp circuit being operable to control the operation when a steady state or DC condition is reached.

Claim 3 (original): The circuit for minimizing the effects of ESD events on data cells of Claim 1, further comprising a data cell with one or a plurality of input nodes responsively coupled to the output of the delay circuit.

Claim 4 (original): The circuit for minimizing the effects of ESD events on data cells of Claim 3, wherein the data cell comprises an EEPROM cell.

Claim 5 (original): The circuit for minimizing the effects of ESD events on data cells of Claim 1, wherein the predetermined voltage threshold is approximately 10 volts.

Claim 6 (currently amended): The circuit for minimizing the effects of ESD events on data cells of Claim 1, wherein the clamp circuit further comprises:

a voltage divider circuit;

a first transistor;

a second transistor;

a third transistor;

a first node;

a second node;

the voltage divider operable to place a voltage on the gate of the first transistor and the source/bulk of the second transistor in the event of an ESD event on the first node;

the second node having a capacitance operable to cause it to rise more slowly during an ESD event;

the gate terminal of the third transistor and the gate of the first transistor being coupled to the second node, operable to cause the gate terminal of the third transistor to be pulled up and the gate of the first transistor to be pulled down as the voltage on the second node rises; and

the first transistor and second transistor being turned off during normal operation when the second node is at approximately five volts.

Claim 7 (original): The circuit for minimizing the effects of ESD events on data cells of Claim 6, wherein the voltage divider further comprises a plurality of resistors being coupled in series.

Claim 8 (original): The circuit for minimizing the effects of ESD events on data cells of Claim 6, wherein the voltage divider is operable to place a voltage between approximately four (4) and six (6) volts on the gate of the first transistor and the source/bulk of the second transistor in the event of a high voltage signal on the first node.

Claim 9 (original): The circuit for minimizing the effects of ESD events on data cells of Claim 6, wherein the transistors comprise MOSFETs.

Claim 10 (previously presented): The circuit for minimizing the effects of ESD events on data cells of Claim 9, further comprising:

the first transistor being an NMOS type; and

the second transistor being a PMOS type.

Claim 11 (original): The circuit for minimizing the effects of ESD events on data cells of Claim 6, wherein the delay circuit further comprises:

a fourth transistor;

a fifth transistor;

a sixth transistor;

a seventh transistor;

a fifth resistor; and

the delay circuit being operable to delay the propagation of a high voltage signal introduced at the first node Vpp.

Claim 12 (original): The circuit for minimizing the effects of ESD events on data cells of Claim 11, wherein the delay circuit further comprises:

a ground reference;

the gate of the fourth transistor and the gate of the fifth transistor being coupled to the ground reference through a large resistance;

the delay circuit operable to cause any rapid voltage rise on the first node Vpp to couple through and pull up the gates of all the transistors, and charge the high resistance path Vpp until the fifth resistor discharges the voltage;

the clamp circuit dominating to provide the dc operating condition required for pulling down one or a plurality of data cell input nodes upon discharge of the fifth resistor; and

the sixth transistor and seventh transistor being operable to slow the voltage rise through the circuit output through an RC time delay.

Claim 13 (original): The circuit for minimizing the effects of ESD events on data cells of Claim 11, wherein the transistors comprises MOSFETs.

Claim 14 (previously presented): The circuit for minimizing the effects of ESD events on data cells of Claim 13, wherein the fourth transistor comprises a PMOS, the fifth transistor comprises a PMOS, the sixth transistor comprises an NMOS and the seventh transistor comprises an NMOS.

Claim 15 (previously presented): The circuit for minimizing the effects of ESD events on data cells of Claim 1, further comprising a CMOS circuit.

Claim 16 (original): The circuit for minimizing the effects of ESD events on data cells of Claim 1, for use in a servo motor controller.

Claim 17 (original): The circuit for minimizing the effects of ESD events on data cells of Claim 16, for use in a computer hard drive controller.

Claim 18 (previously presented): A circuit for shunting high voltage signals, comprising:

a clamp circuit with an input and output to clamp after an ESD event;

a delay circuit with an input and an output to delay during said ESD event;

the output of the clamp circuit responsively coupled to the input of the delay circuit; and

the coupled clamp circuit and delay circuit operable to shunt voltage above a certain threshold to ground.

Claim 19 (previously presented): The circuit for shunting high voltage signals of Claim 18, further comprising a CMOS circuit.

Claim 20 (original): The circuit for shunting high voltage signals of Claim 18, for use in a servo motor controller.

Claims 21-26 (cancelled).